A 4.0 WATT HIGH EFFICIENCY 15-18 GHZ POWER MMIC

M. Gat, D. S. Day and J. R. Basset

Microwave Power Products
Avantek Inc.,
3175 Bowers Ave.,
Santa Clara, CA 95054

ABSTRACT

A two-stage Ku-band monolithic power amplifier is reported. The MMIC incorporates a full interstage matching network and partial input matching network on the chip. The amplifier delivers 4 watts of power, 10 to 13 dB of gain and more than 20% power added efficiency at 2 dB gain compression. This amplifier can be tuned for a 1 GHz instantaneous bandwidth anywhere in the 15-18 GHz band. To the best of our knowledge, the combination of output power, power-added efficiency and gain are the best published results for a power MMIC operating at 18 GHz to date.

INTRODUCTION

In recent years power MMICs covering the C, S and X-bands have gained acceptance as building blocks for power amplifiers. Published MMIC results at Ku-band have so far been limited to low power levels, low efficiency and narrow bandwidth [1,2]. This paper presents an MMIC with substantial improvements in power levels (4 watts) and bandwidth (15-18 GHz), coupled with high power-added efficiency (>20%) and substantial gain (10 to 13 dB). Thus, this work extends the usefulness of power MMICs into Ku band.

The need for ever increasing power, coupled with relatively fixed power density levels presents the designer with a dilemma. At question is the 'optimal' size of a building block, weighing the desirability of reducing parts count against the need for acceptable yields. Avantek's design approach uses two-stage MMIC gain blocks which incorporate full on-chip interstage matching networks and partial on-chip input matching networks, with the rest of the matching realized external to the chip. The benefits of this approach which include high efficiency, high gain and low cost, have been discussed in detail previously [3,4,5]. A 3- to 4-watt building block of this configuration seems an optimal device for Ku-band power modules. The MMIC size is small, but the power density is still high and at least two MMICs could be easily combined in parallel with low combining loss.

A power amplifier module which uses five of these modules as building blocks was built [6]. This module illustrates the usefulness of the MMIC. The module delivers 10 watts of power, 14% power-added efficiency and 20 dB of gain at 18 GHz. The module can be used for both CW and pulsed applications. For short-pulse operation (< 50 μs), 0.5 to 1.0 dB more power output is expected.

CIRCUIT DESIGN

The MMIC uses a 4.22-mm FET driving an 8.45-mm FET. The size of the output FET was chosen based on empirical data and a minimum power density of 400 mW/mm. The driver-to-output stage ratio of 2:1 was based on empirical data and referenced to the minimum requirement that the ratio be less than $10\,exp[(gain\text{-}loss)/10]$. Both FETs are constructed of cells of 8 gate fingers. Each gate finger is 66 μm wide. The output FET has 16 cells, totaling 128 fingers. The driver FET is split into four equal parts, each consists of two cells. The number of cells was intentionally kept as a binary number to facilitate easy power combining and splitting. Detailed information on the FET structure and MMIC fabrication have been published previously [3,4,5]. The layout of the MMIC is shown in Figure 1.

The output matching network is realized off-chip on a 5-mil alumina substrate, using an N=2 binary tree topology. Balancing resistors are printed on the low impedance arms of the network. The output matching network is wideband in nature due to the relatively low Q of the output FET. The DC drain current is injected via a 0.25-λ shorted stub that also serves as an RF short for the second harmonic. The 16 FET

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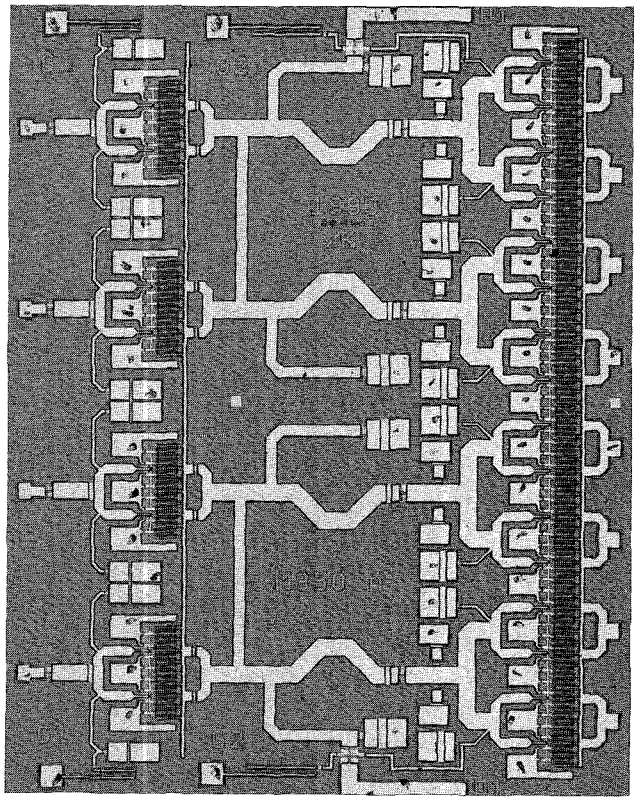

Figure 1. Micrograph of Ku-Band MMIC

cells are combined in pairs to form eight output bonding pads. The number of output pads was not reduced any further because of a limitation on the minimum inductance of the output bond wires.

The design of the interstage matching network is the most important and time-consuming part of the MMIC design process. The application of the Fano-Bode bandwidth limit to the large signal model of the two FETs revealed that for the required bandwidth "de-'Q'ing" is not needed. Consequently, a purely reactive matching network is employed to maximize gain and efficiency. A simplified schematic of the matching network is shown in figure 2. All parts of the matching network are elements which are needed for power combining and splitting, DC blocking and DC injection. The only exceptional 'extra element' is the shunt capacitor that forms an impedance transformer with the DC block. Therefore, the network is 'minimal' from a layout view point. The interstage matching network was clustered into four segments with identical RF characteristics. The need to keep the shunt capacitor close to the gate of the output FET necessitates clustering. The DC drain current for the driver FETs is injected from both sides of the MMIC to keep current density low, well away from the electro-migration range. The gates and the drains of the four driving FETs are connected to avoid odd-mode oscillations [7].

The input matching network starts on-chip with a DC block and a shunt L-C pre-match. The shunt pre-match capacitors of the four driving FETs are connected to route V_{gs} from the bonding pad. The shunt L-C pre-match transforms the low input impedance of the FETs, thus enabling the realization of the external matching network on a 5-mil alumina substrate. The external input matching network is an N=2 binary tree.

Five different revisions were realized on the mask. The five revisions have identical layouts but different capacitor values in the interstage matching network. Scaling the capacitor values shifts the frequency response of the network. Dimensions of the MMIC die are 0.081" x 0.104" x 0.003".

PERFORMANCE

The MMICs were tested in a 50Ω system with no external tuners. All measured data were taken at 25° C under CW operation. Bias voltage was set at +9 V with I_{dsq} of 30%-40% I_{dss}. Launcher losses were not de-embedded. Figure 3 shows typical performance of the best layout (revision "E") at 2 dB gain compression, tuned to the 16-18 GHz range. The power ranges from +35.5 to +36.6 dBm, which corresponds to a power density of 420-530 mW/mm for the power stage. The power-added efficiency varies between 23% and 30% and the associated gain is 10-13 dB. Figure 4 shows a low frequency version (revision "C") tuned to the 14.5-15.5 GHz range. Figure 5 shows the performance of the best MMIC: +37 dBm of power, 10 dB of gain and 29% PAE at 18 GHz.

Thermal measurements of the MMICs were done using the liquid crystal method and verified using an IR microscope. The temperature of the hottest point on the MMIC is 73 °C above the flange temperature and the thermal resistance was R_{th}= 82 mm(°C/W). Though the measurements were done using CW signals, most of these MMICs are used for short pulse applications (<50 μs), where the power and the gain are expected to be 0.5 to 1.0 dB higher.

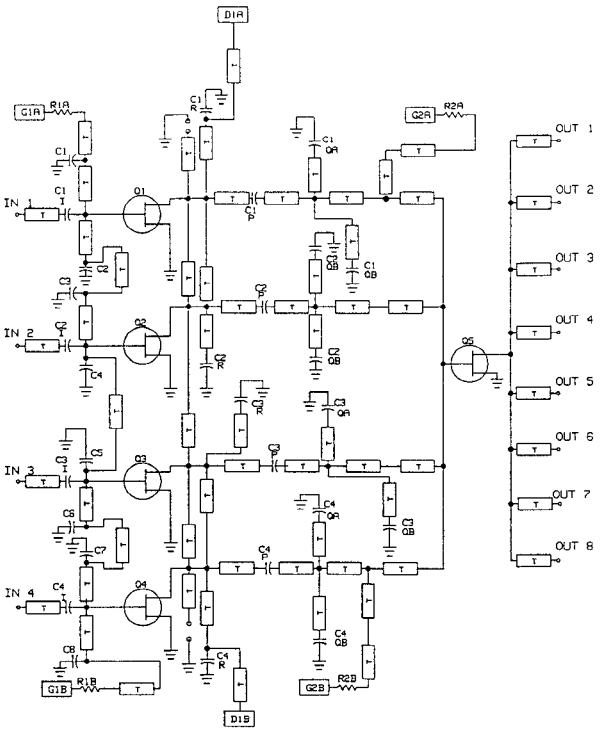

Figure 2. MMIC Simplified Schematic

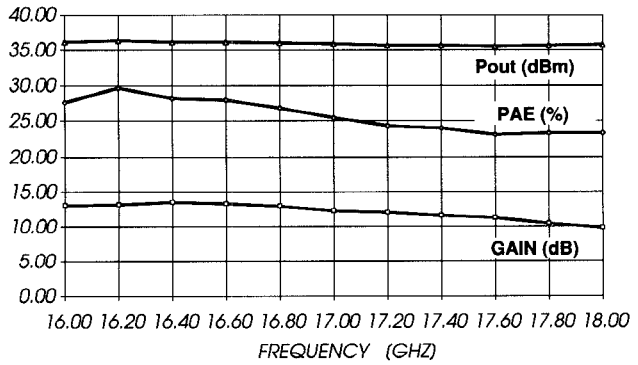

Figure 3. Typical MMIC Response at 2 dB Gain Compression

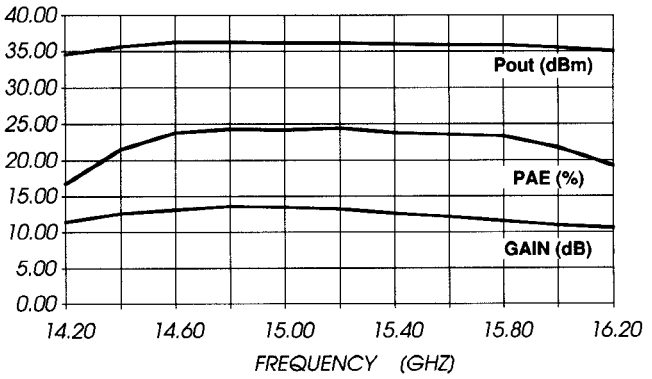

Figure 4. 14-16 GHz MMIC Response at 2 dB Gain Compression

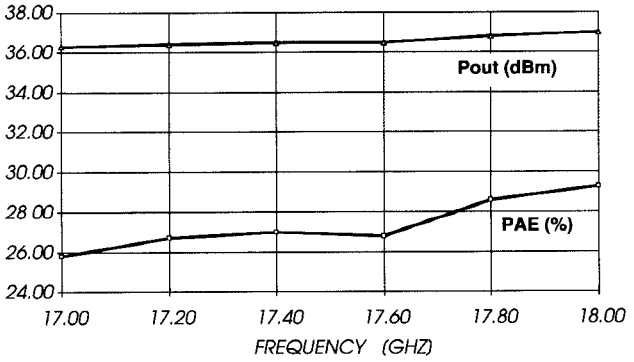

Figure 5. Best MMIC Response at 2 dB Gain Compression

CONCLUSION

A Ku-band power MMIC has been demonstrated. High power added efficiency and large bandwidth, coupled with Avantek's partial match approach resulted in a useful and yet relatively small MMIC. A 10-watt, 20-dB gain power module using five MMICs demonstrates the usefulness of the MMIC as a building block for higher-power amplifiers. It is expected that the MMIC, due to its superior performance, will replace discrete FETs in future power amplifiers.

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